

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions  
and listings of claims in the application:

Listing of Claims:

C<sup>21</sup> 1        1. (Previously Amended) A semiconductor device,  
2 comprising:  
3              a semiconductor region formed in a semiconductor  
4 substrate;  
5              a plurality of basic cells regularly arranged on said  
6 semiconductor substrate;  
7              a plurality of field effect transistors arranged in  
8 each of a plurality of said basic cells and formed in said  
9 semiconductor region;  
10          power supply wirings arranged for supplying power  
11 supply voltages to a plurality of said field effect  
12 transistors; and  
13          switch elements provided between said semiconductor  
14 region and said power supply wirings,  
15          wherein said switch elements include field effect  
16 transistors of said basic cells.

Claims 2 - 6 (Cancelled)

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1       7. (Currently Amended) A semiconductor device,  
2 comprising:  
3           a semiconductor region formed in a semiconductor  
4 substrate;  
5           a plurality of basic cells regularly arranged on said  
6 semiconductor substrate;  
7           a plurality of field effect transistors arranged in  
8 each of a plurality of said basic cells and formed in said  
9 semiconductor region;  
10          power supply wirings arranged for supplying the power  
11 supply voltages to a plurality of said field effect  
12 transistors; and  
13          switch elements provided between said semiconductor  
14 region and said power supply wirings;  
15          wherein said switch elements are formed of the include  
16 field effect transistors in of said basic cells and are  
17 discretely arranged in said semiconductor region.

1       8. (Currently Amended) A semiconductor device,  
2 comprising:

C<sup>31</sup> 3        a semiconductor region formed in a semiconductor  
4        substrate;  
  
5        a plurality of basic cells regularly arranged in on  
6        said semiconductor substrate;  
  
7        a plurality of field effect transistors arranged in  
8        each of a plurality of said basic cells and formed in said  
9        semiconductor region;  
  
10      power supply wirings arranged for supplying the power  
11      supply voltages to said field effect transistors; and  
  
12      switch elements provided between said semiconductor  
13      region and said power supply wirings,  
  
14      wherein said switch elements are formed of include  
15      field effect transistors of said basic cells, and wherein a  
16      semiconductor region, which is formed within said  
17      semiconductor region in a plurality of said basic cells,  
18      and of the a conductivity type opposed to that of said  
19      semiconductor region, and is electrically connected to said  
20      power supply wirings are electrically connected.

1        9. (Currently Amended) A semiconductor device,  
2        comprising:  
  
3        a semiconductor region formed in a semiconductor  
4        substrate;

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5        a plurality of basic cells regularly arranged on said  
6        semiconductor substrate;

7        a plurality of field effect transistors arranged in  
8        each of a plurality of basic cells and are formed in said  
9        semiconductor region;

10      power supply wirings arranged for supplying the power  
11      supply voltages to said field effect transistors; and  
12      switch elements provided between said semiconductor  
13      region and said power supply wirings,  
14      wherein said switch elements are formed of the include  
15      field effect transistors of said basic cells, and at least  
16      one of a pair of semiconductor regions for source and drain  
17      of unused field effect transistors of said field effect  
18      transistors and said power supply wirings are electrically  
19      connected.

1        10. (Currently Amended) A semiconductor device,  
2        comprising:  
3        a semiconductor region formed in a semiconductor  
4        substrate;  
5        a plurality of basic cells regularly arranged in on  
6        said semiconductor substrate;  
7        a plurality of field effect transistors arrang d in

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8 each of a plurality of said basic cells and formed in said  
9 semiconductor region;

10 power supply wirings arranged for supplying the power  
11 supply voltages to said field effect transistors; and  
12 switch elements provided between said semiconductor  
13 region and said power supply wirings,

14 wherein said switch elements are formed of said  
15 include field effect transistors of said basic cells and  
16 are discretely arranged within said semiconductor region,  
17 and

18 wherein a semiconductor region, formed in said  
19 semiconductor region of a plurality of basic cells, and of  
20 the a conductivity type opposed to that of said  
21 semiconductor region, and said power supply wirings are  
22 electrically connected.

1 11. (Currently Amended) A semiconductor device,  
2 comprising:  
3 a semiconductor region formed in a semiconductor  
4 substrate;  
5 a plurality of basic cells regularly arranged in on  
6 said semiconductor substrate;

C<sup>3\</sup> 7        a plurality of field effect transistors arranged in  
8        each of a plurality of said basic cells and are formed in  
9        said semiconductor region;  
10        power supply wirings arranged for supplying the power  
11        supply voltages to said field effect transistors; and  
12        switch elements provided between said semiconductor  
13        region and said power supply wirings,  
14        wherein said switch elements are formed of said  
15        include field effect transistors of said basic cells and  
16        are discretely arranged within said semiconductor region,  
17        and  
18        wherein at least one of a pair of semiconductor  
19        regions for source and drain of unused field effect  
20        transistors of said field effect transistors and said power  
21        supply wirings are electrically connected.

1        12. (Currently Amended) A semiconductor device,  
2        comprising:  
3        a semiconductor region formed in a semiconductor  
4        substrate;  
5        a plurality of basic cells regularly arranged in on  
6        said semiconductor substrate;

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7           a plurality of field effect transistors arranged in  
8    each of a plurality of said basic cells and formed in said  
9    semiconductor region;  
10          power supply wirings arranged for supplying the power  
11    supply voltages to said field effect transistors; and  
12          switch elements provided between said semiconductor  
13    region and said power supply wirings,  
14          wherein said switch elements are formed of said  
15    include field effect transistors of said basic cells and  
16    are discretely arranged in said semiconductor region, and  
17          wherein at least one of a pair of semiconductor  
18    regions for source and drain of unused field effect  
19    transistors arranged between the switch elements discretely  
20    arranged in said semiconductor region among said field  
21    effect transistors and said power supply wirings are  
22    electrically connected.

1           13. (Currently Amended) A semiconductor device,  
2    comprising:  
3          a semiconductor region formed in a semiconductor  
4    substrate;  
5          a plurality of basic cells regularly arranged in on  
6    said semiconductor substrate;

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7        a plurality of field effect transistors arranged in  
8    each of a plurality of said basic cells and formed in said  
9    semiconductor region;  
10      circuits formed of a plurality of said basic cells;  
11      power supply wirings arranged for supplying the power  
12    supply voltages to said field effect transistors; and  
13      switch elements provided between said semiconductor  
14    region and said power supply wirings,  
15      wherein said switch elements are built in the a  
16    predetermined circuit among said circuits.

1        14. (Currently Amended) A semiconductor device,  
2   comprising:  
3        a semiconductor region formed in a semiconductor  
4   substrate;  
5        a plurality of basic cells regularly arranged in on  
6   said semiconductor substrate;  
7        a plurality of field effect transistors arranged in  
8   each of a plurality of said basic cells and formed in said  
9   semiconductor region;  
10      circuits formed of a plurality of said basic cells;  
11      power supply wirings arranged for supplying the power  
12    supply voltages to said field effect transistors; and

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13        switch elements provided between said semiconductor  
14        region and said power supply wirings,

15        wherein said circuits include the a circuit to in  
16        which said switch elements are built in and the a circuit  
17        to in which said switch elements are not built in.

1            15. (Currently Amended) A semiconductor device as  
2        claimed in claim 13 or 14, wherein a semiconductor region,  
3        ~~of the conductivity type opposed to that of said~~  
4        ~~semiconductor region, formed in said semiconductor region~~  
5        ~~of a plurality of said basic cells and of a conductivity~~  
6        ~~type opposed to that of said semiconductor region, and said~~  
7        power supply wirings are electrically connected.

1            16. (Original) A semiconductor as claim in claim 13  
2        or 14, wherein at least one of a pair of semiconductor  
3        regions for source and drain of unused field effect  
4        transistors among said field effect transistors and said  
5        power supply wirings are electrically connected.

1            17. (Previously Amended) A semiconductor device as  
2        claimed in claim 13 or 14, wherein said circuits are logic  
3        circuits and said switch elements are discretely arranged

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4 in said semiconductor substrate.

1           18. (Original) A semiconductor device as claimed in  
2 claim 16, wherein said unused field effect transistors are  
3 field effect transistors of basic cells not forming logic  
4 circuits and said unused basic cells are formed among said  
5 switch elements.

1           19. (Currently Amended) A semiconductor device as  
2 claimed in claim 13 or 14, wherein said circuit comprising  
3 in which the switch elements are built in is a clock  
4 circuit or a flip-flop circuit.

1           20. (Currently Amended) A semiconductor device as  
2 claimed in claim 13 or 14, wherein said switch elements are  
3 formed of include field effect transistors in of said basic  
4 cells.

1           21. (Currently Amended) A semiconductor device as  
2 claimed in any one of claims 7 to 14, wherein said basic  
3 cells include the p-channel type field effect transistors  
4 and n-channel type field effect transistors.

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1        22. (Previously Amended) A semiconductor device as  
2        claimed in any one of claims 7 to 12, further comprising:  
3              a first wiring layer formed over said switch elements;  
4              a second wiring layer formed over said first wiring  
5        layer and having wiring extending in a direction transverse  
6        to wiring of said first wiring layer; and  
7              a third wiring layer formed over said second wiring  
8        layer and having wiring extending in a direction transverse  
9        to wiring of said second wiring layer,  
10          wherein a wiring electrically connected to gate  
11        electrodes of said switch elements is formed of wiring of  
12        the third wiring layer and arranged in parallel to said  
13        power supply wirings.

1        23. (Previously Amended) A semiconductor device as  
2        claimed in any one of claims 7 to 14, wherein a  
3        semiconductor region for power feeding to supply a  
4        predetermined voltage to the semiconductor region formed in  
5        said semiconductor substrate is formed in a region between  
6        an internal circuit region where a plurality of said basic  
7        cells are arranged and a peripheral circuit region at an  
8        external side of said internal circuit region.

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1        24. (Original) A semiconductor device as claimed in  
2        claim 23, wherein a wiring for supplying the predetermined  
3        voltage to said semiconductor region for power feeding is  
4        arranged to surround said internal circuit region.

1        25. (Currently Amended) A semiconductor device as  
2        claimed in claim 24, wherein the wiring for supplying the  
3        predetermined voltage to said semiconductor region for  
4        power feeding is electrically connected to the a terminal  
5        for testing via the an external terminal of the  
6        semiconductor device.

1        26. (Currently Amended) A semiconductor device as  
2        claimed in claim 24, wherein the wiring for supplying the  
3        predetermined voltage to said semiconductor region for  
4        power feeding is electrically connected to the wiring for  
5        power feeding arranged like a lattice within said internal  
6        circuit region.

1        27. (Currently Amended) A semiconductor device as  
2        claimed in any one of claims 1 and 7 to 14, wherein said  
3        switch elements are turned ON in the a normal operation  
4        period of the semiconductor device and the a power supply

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5      voltage is applied from said power supply wirings to the  
6      semiconductor region formed in said semiconductor  
7      substrate, and said switch elements are turned OFF in the a  
8      testing or waiting period of the semiconductor device and  
9      the a voltage different from said power supply voltage is  
10     applied to said semiconductor region.

1            28. (Currently Amended) A semiconductor device,  
2      comprising:  
3                a first semiconductor region formed in a semiconductor  
4      substrate;  
5                a second semiconductor region formed in said  
6      semiconductor substrate to have a conductivity type opposed  
7      to that of said first semiconductor region;  
8                a plurality of basic cells regularly arranged in on  
9      said semiconductor substrate;  
10          a first field effect transistors formed in said first  
11      semiconductor region as the field effect transistors of  
12      said basic cells;  
13          a second field effect transistors formed in said  
14      second semiconductor region as the field effect transistors of  
15      said basic cells and to have the a conductivity type  
16      opposed to that of said first field effect transistors;

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17        a first power supply wiring connected to said first  
18        field effect transistors;  
  
19        a second power supply wiring connected to said second  
20        field effect transistors to supply a potential which is  
21        relatively lower than the a potential of said first power  
22        supply wiring;  
  
23        first switch elements provided between said first  
24        semiconductor region and said first power supply wiring;  
25        and  
  
26        second switch elements provided between said second  
27        semiconductor region and said second power supply wiring,  
28        wherein said first switch elements are formed of the  
29        first field effect transistors in said basic cells and  
30        discretely arranged within said first semiconductor region,  
31        and  
  
32        wherein said second switch elements are formed of the  
33        second field effect transistors in said basic cells and  
34        discretely arranged within said second semiconductor  
35        region.

1            29. (Currently Amended) A semiconductor device,  
2        comprising:

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3        a first semiconductor region formed in a semiconductor  
4        substrate;

5        a second semiconductor region formed in said  
6        semiconductor substrate to have a conductivity type opposed  
7        to that of said first semiconductor region;

8        a plurality of basic cells regularly arranged in on  
9        said semiconductor substrate;

10      a first field effect transistors  formed in said first  
11      semiconductor region as the field effect transistors in of  
12      said basic cells;

13      a second field effect transistors, as the field effect  
14      transistor in said basic cells, formed in said second  
15      semiconductor region as field effect transistors of said  
16      basic cells and to have the a conductivity type opposed to  
17      that of said first field effect transistors;

18      a first power supply wiring connected to said first  
19      field effect transistors;

20      a second power supply wiring connected to said second  
21      field effect transistors  to supply the a potential which is  
22      relatively lower than that of said first power supply  
23      wiring;

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24        a first switch elements provided between said first  
25    semiconductor region and said first power supply wiring;

26    and

27        a second switch elements provided between said second  
28    semiconductor region and said second power supply wiring,

29        wherein said first switch elements include is formed  
30    of the first field effect transistors in the predetermined  
31    basic cells among a said plurality of said basic cells,

32        wherein said second switch elements include is formed  
33    of the second field effect transistors in the predetermined  
34    basic cells among a said plurality of said basic cells,

35        wherein the a region formed in said first  
36    semiconductor region in a plurality of said basic cells  
37    electrically connects the semiconductor region of the  
38    conductivity type opposed to that of said first  
39    semiconductor region and said first power supply wiring,

40    and

41        wherein the a region formed in said second  
42    semiconductor region in a plurality of basic cells  
43    electrically connects the semiconductor region of the  
44    conductivity type opposed to that of said second  
45    semiconductor region and said second power supply wiring.

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1       30. (Currently Amended) A semiconductor device,  
2 comprising:  
3            a first semiconductor region formed in a semiconductor  
4            substrate;  
5            a second semiconductor region formed in said  
6            semiconductor substrate to have a conductivity type opposed  
7            to that of said first semiconductor region;  
8            a plurality of basic cells regularly arranged in on  
9            said semiconductor substrate;  
10          a first field effect transistorss formed in said first  
11          semiconductor region as the field effect transistorss of  
12          said basic cells;  
13          a second field effect transistorss, ~~as the field effect~~  
14          transistor of said basic cells, formed in said second  
15          semiconductor region as field effect transistors of said  
16          basic cells and to have the a conductivity type opposed to  
17          that of said first field effect transistors;  
18          a first power supply wiring connected to said first  
19          effect transistors;  
20          a second power supply wiring connected to said second  
21          field effect transistorss to supply the a potential  
22          relatively lower than that of said first power supply  
23          wiring;

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24        a first switch elements provided between said first  
25    semiconductor region and said first power supply wiring;  
26    and  
  
27        a second switch elements provided between said second  
28    semiconductor region and said second power supply wiring,  
  
29        wherein said first switch elements include is formed  
30    of the first field effect transistors in the predetermined  
31    basic cells among a said plurality of said basic cells,  
  
32        wherein said second switch elements include is formed  
33    of the second field effect transistors in the predetermined  
34    basic cells among a said plurality of said basic cells,  
  
35        wherein at least one of a pair of semiconductor  
36    regions for source and drain of unused first field effect  
37    transistors among said first field effect transistors is  
38    electrically connected to said first power supply wiring,  
39    and  
  
40        wherein at least one of a pair of semiconductor  
41    regions for source and drain of unused second field effect  
42    transistors among a plurality of said second field effect  
43    transistors is electrically connected said second power  
44    supply wiring.

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1       31. (Currently Amended) A semiconductor device,  
2 comprising:  
3            a first semiconductor region formed in a semiconductor  
4            substrate;  
5            a second semiconductor region formed in said  
6            semiconductor substrate to have the a conductivity type  
7            opposed to that of said first semiconductor region;  
8            a plurality of basic cells regularly arranged in on  
9            said semiconductor substrate;  
10          a first field effect transistors formed in said first  
11          semiconductor region as the field effect transistors of  
12          said basic cells;  
13          a second field effect transistors formed, ~~as the field~~  
14          ~~effect transistor of said basic cell,~~ in said second  
15          semiconductor region as field effect transistors of said  
16          basic cells and to have the a conductivity type opposed to  
17          that of said first field effect transistors;  
18          a first power supply wiring connected to said first  
19          field effect transistors;  
20          a second power supply wiring connected to said second  
21          field effect transistors to supply the a potential  
22          relatively lower than that of said first power supply  
23          wiring;

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24        a first switch elements provided between said first  
25    semiconductor region and said first power supply wiring;  
26    and  
  
27        a second switch elements provided between said second  
28    semiconductor region and said second power supply wiring,  
  
29        wherein said first switch elements include are formed  
30    of the first field effect transistors in the predetermined  
31    basic cells among a said plurality of said basic cells and  
32    are discretely arranged in said first semiconductor region,  
  
33        wherein said second switch elements include are formed  
34    of the second field effect transistors in the predetermined  
35    basic cells among a said plurality of said basic cells and  
36    are discretely arranged in said first second semiconductor  
37    region,  
  
38        wherein the a region formed in said first  
39    semiconductor region in a plurality of said basic cells  
40    electrically connects the semiconductor region of the  
41    conductivity type opposed to that of said first  
42    semiconductor region and said first power supply wiring,  
43    and  
  
44        wherein the a region formed in said second  
45    semiconductor region in a plurality of said basic cells  
46    electrically connects the semiconductor region of th

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47 conductivity type opposed to that of said second  
48 semiconductor region and said second power supply wiring.

1           32. (Currently Amended) A semiconductor device,  
2 comprising:  
3           a first semiconductor region formed in a semiconductor  
4 substrate;  
5           a second semiconductor region formed in said  
6 semiconductor substrate to have the a conductivity type  
7 opposed to that of said first semiconductor region;  
8           a plurality of basic cells regularly arranged in on  
9 said semiconductor substrate;  
10          a first field effect transistors formed in said first  
11 semiconductor region as the field effect transistors of  
12 said basic cells;  
13          a second field effect transistors formed, ~~as the field~~  
14 ~~effect transistor of said basic cells,~~ in said second  
15 semiconductor region as field effect transistors of said  
16 basic cells and to have the channel of the conductivity  
17 type opposed to that of said first field effect  
18 transistors;  
19          a first power supply wiring connected to said first  
20 field effect transistors;

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21        a second power supply wiring connected to said second  
22        field effect transistors to supply the a potential  
23        relatively lower than that of said first power supply  
24        wiring;

25        a first switch elements provided between said first  
26        semiconductor region and said first power supply wiring;  
27        and

28        a second switch elements provided between said second  
29        semiconductor region and said second power supply wiring,

30        wherein said first switch elements include are formed  
31        of the first field effect transistors in the predetermined  
32        basic cells among a said plurality of basic cells and are  
33        discretely arranged in said first semiconductor region,

34        wherein said second switch elements include are formed  
35        of the second field effect transistors in the predetermined  
36        basic cells among a said plurality of basic cells and are  
37        discretely arranged in said first second semiconductor  
38        region,

39        wherein at least one of a pair of semiconductor  
40        regions for source and drain of unused first field effect  
41        transistors among a plurality of said first field effect  
42        transistors is lectrically connected to said first power  
43        supply wiring, and

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44 wherein at least one of a pair of semiconductor  
45 regions for source and drain of unused second field effect  
46 transistors among a plurality of said second field effect  
47 transistors is electrically connected to said second power  
48 supply wiring.

1       33. (Currently Amended) A semiconductor device,  
2 comprising:  
3       first and second semiconductor regions formed in the a  
4 peripheral circuit region of a semiconductor substrate;  
5       a plurality of cells for input/output circuits  
6 regularly arranged in the peripheral circuit region of said  
7 semiconductor substrate;  
8       a plurality of field effect transistors for  
9 input/output circuits arranged in each of a plurality of  
10 cells for input/output circuits and formed in said first  
11 and second semiconductor regions;  
12       power supply wiring arranged for supplying the a power  
13 supply voltage to a plurality of said field effect  
14 transistors for input/output circuits; and  
15       switch elements provided between the second  
16 semiconductor region in said p ripheral circuit region and  
17 said power supply wiring,

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18 wherein an output circuit electrically connected to  
19 the an external terminal includes is formed of the field  
20 effect transistors for input/output circuits in said first  
21 semiconductor region and an input circuit electrically  
22 connected to the an external terminal includes is formed of  
23 the field effect transistors for input/output circuits in  
24 said second semiconductor region, and  
25 wherein said switch elements include are formed of the  
26 field effect transistors not used for the input circuit  
27 among the field effect transistors for input/output  
28 circuits in said second semiconductor region.

1 34. (Currently Amended) A semiconductor device,  
2 comprising:  
3 a semiconductor region formed in the a peripheral  
4 circuit region of a semiconductor substrate;  
5 a plurality of cells for input/output circuits  
6 regularly arranged in the peripheral circuit region of said  
7 semiconductor substrate;  
8 a plurality of field effect transistors for  
9 input/output circuits arranged in each of a plurality of  
10 cells for input/output circuits and formed in said  
11 semiconductor region;

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12 power supply wiring arranged for supplying the a power  
13 supply voltage to a plurality of said field effect  
14 transistors for input/output circuits; and  
15 switch elements provided between the semiconductor  
16 region in said peripheral circuit region and said power  
17 supply wiring,  
18 wherein said peripheral circuit region includes an  
19 external region to arrange said field effect transistors  
20 for input/output circuits of relatively higher threshold  
21 voltage and an internal region to arrange said field effect  
22 transistors for input/output circuits of relatively lower  
23 threshold voltage, and  
24 wherein said switch elements include is formed of the  
25 field effect transistors not used for input circuit among  
26 the field effect transistors for input/output circuits in  
27 said internal region.

1 35. (Currently Amended) A semiconductor device as  
2 claimed in claim 34, wherein an output circuit includes a  
3 is formed of the field effect transistor for input/output  
4 circuits in said external region and an input circuit  
5 includes a is formed of the field effect transistor for  
6 input/output circuits in said internal region.

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1           36. (Currently Amended) A semiconductor device as  
2       claimed in claim 33, 34 or 35, wherein the a gate  
3       insulation film of the field effect transistor forming of  
4       said output circuit is thicker than the a gate insulation  
5       film of the field effect transistor forming of said input  
6       circuit.

1           37. (Currently Amended) A semiconductor device as  
2       claimed in claim 33, 34, or 35, wherein the wiring  
3       connected to the gate electrodes of the field effect  
4       transistors of forming said switch elements is arranged to  
5       surround the said internal circuit region of a  
6       semiconductor device.

1           38. (Previously Amended) A semiconductor device as  
2       claimed in any one of claims 33 to 35, wherein at least one  
3       of a pair of semiconductor regions for source and drain of  
4       the field effect transistors unused for said input/output  
5       circuits is electrically connected to said power supply  
6       wiring to form a capacitance element.

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1        39. (Currently Amended) A method of manufacturing a  
2    semiconductor device, comprising ~~the processes of:~~  
3            (a) regularly allocating a plurality of basic cells  
4    on a semiconductor substrate;  
5            (b) forming a switch element arranged for  
6    electrically connecting ~~or~~ and disconnecting ~~the a~~  
7    semiconductor region formed on said semiconductor substrate  
8    and ~~the a~~ power supply wiring of the semiconductor device  
9    with field effect transistors of predetermined basic cells  
10   among said plurality of basic cells; and  
11           (c) forming a plurality of circuits with the  
12   predetermined basic cells among a said plurality of said  
13   basic cells.

1        40. (Currently Amended) A method of manufacturing a  
2    semiconductor device, comprising ~~the processes of:~~  
3            (a) regularly allocating a plurality of basic cells  
4    on a semiconductor substrate;  
5            (b) forming a switch elements arranged for  
6    electrically connecting and disconnecting ~~the a~~  
7    semiconductor region formed on said semiconductor substrate  
8    and ~~the a~~ power supply wiring of the semiconductor device

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9       with the field effect transistors of the predetermined  
10      basic cells among a said plurality of said basic cells;  
11           (c) forming a plurality of circuits with the  
12      predetermined basic cells among a said plurality of said  
13      basic cells; and  
14           (d) allocating a contact hole arranged for  
15      electrically connecting at least one of a pair of  
16      semiconductor regions for source and drain of unused field  
17      effect transistors among a plurality field effect  
18      transistors of said basic cells and said power supply  
19      wiring.

1           41. (Currently Amended) A method of manufacturing a  
2      semiconductor device, comprising the processes of:  
3           (a) regularly allocating a plurality basic cells on a  
4      semiconductor substrate;  
5           (b) forming a switch element arranged for  
6      electrically connecting and disconnecting the a  
7      semiconductor region formed on said semiconductor substrate  
8      and the a power supply wiring of the semiconductor device  
9      with the a field effect transistor of the a predetermined  
10     basic cells among a said plurality of said basic cells; and

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11           (c) forming a plurality of circuits with the  
12 predetermined basic cells among a said plurality of basic  
13 cells,

14           wherein said switch element is built in the a  
15 predetermined circuit among a said plurality of said  
16 circuits in said process step (c).

1           42. (Currently Amended) A method of manufacturing a  
2 semiconductor device, comprising the processes of:

3           (a) regularly allocating a plurality of basic cells  
4 on a semiconductor substrate; and  
5           (b) forming a plurality of circuits with the  
6 predetermined basic cells among a said plurality of said  
7 basic cells,

8           wherein said a switch element is built in the a  
9 predetermined circuit among a plurality of said circuits,

10           said switch element including a field effect  
11 transistor of a basic cell of said predetermined circuit  
12 and being provided between a power supply wiring and a  
13 semiconductor region in which field effect transistors of  
14 other basic cells of said predetermined circuit are formed.

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1       43. (Currently Amended) A semiconductor device as  
2       claimed in claim 2, 4, 6 or 8, wherein a capacitance  
3       element is formed of said semiconductor region and a  
4       semiconductor region of the a conductivity type opposed to  
5       that of said semiconductor region.

1       44. (Currently Amended) A semiconductor device as  
2       claimed in claim 3, 5, 9, 11 or 12, wherein a capacitance  
3       element is formed of said semiconductor region and at least  
4       one of a pair of semiconductor regions for source and drain  
5       of said unused field effect transistors.

1       45. (Currently Amended) A semiconductor device as  
2       claimed in any one of claims 7 to 12, wherein a logic  
3       circuit is formed using said basic cells and said logic  
4       circuit is formed among the basic cells forming including  
5       said switch elements.

1       46. (Currently Amended) A semiconductor device  
2       claimed in claim 9, 11, or 12, wherein a logic circuit is  
3       formed using said basic cells, said unused a field effect  
4       transistor having said one pair of semiconductor regions is  
5       the a field effect transistor of an unused basic cell not

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6 forming a logic circuit, and said logic circuit and unused  
7 basic cells are formed among the basic cells forming  
8 including said switch elements.

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